STATIC INDUCTION SEMICONDUCTOR DEVICE WITH A DISTRIBUTED MAIN ELECTRODE STRUCTURE AND STATIC INDUCTION SEMICONDUCTOR DEVICE WITH A STATIC INDUCTION MAIN ELECTRODE SHORTED STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of power semiconductor device and, more particularly, to a static induction semiconductor device with a distributed main electrode structure which is improved in the device turn-off performance through substantial reduction of the minority carrier storage time, the device fall time and the quantity of gate electrode pull-out charges that are factors important to the turn-off switching performance of the device. The invention also pertains to a static induction semiconductor device with a static induction main electrode shorted structure which permits reduction of the quantity of charges that are pulled out of the gate electrode when the device is turned off.

2. Description of the Prior Art

There have heretofore been proposed a variety of structures intended to improve switching performance of static induction (hereinafter abbreviated to SI) semiconductor devices. FIG. **43** shows in section the structure of a first prior art example that is proposed by Nishizawa and Tamamushi in Japanese Patent Public Disclosure No. 91474/89 to reduce the input capacitance between the gate and the source or between the gate and the cathode and enhance the efficiency of electron injection from the source or cathode region in an SI transistor or thyristor with a buried gate structure. In FIG. **43**, reference numeral **1** denotes an n^--type high resistivity layer, **3** an anode or drain region, **4** gate regions, **5** channel regions and **11** cathode or source regions.

In the first prior art example, a semiconductor region that serves as a cathode or source is provided only above a channel defined by buried gates therebetween to reduce the capacitance between the gate-cathode or gate-source capacitance to thereby increase the device switching speed with no reduction of the channel current.

Since the semiconductor region of high impurity concentration, which serves as the cathode or source region, is provided only above the channel region defined by the buried gate regions therebetween, the junction capacitance between the gate and cathode or source regions is smaller than in the past. Accordingly, a time constant that is defined by the product of the gate resistance and the junction capacitance is smaller than before and the gate-cathode or gate-source voltage reaches the gate region apart from a gate electrode more rapidly than before. This reduces the turn-on time and the turn-off time, and hence permits high-speed switching of the device.

A second prior art example is shown in FIG. **44**, which is a sectional view of an SI thyristor disclosed by Kawamura and Morikawa in Japanese Patent Public Disclosure No. 257266/90. In FIG. **44**, reference numeral **1** denotes an n^--type high resistivity layer, **3** p^+-type anode regions, **4** gate regions, **6** n^+-type short-circuit layers, *7a* a cathode electrode, *7b* a gate electrode, *7c* an anode electrode, **11** n^+-type cathode regions and **13** p^+type short-circuit regions. The structure depicted in FIG. **44** is intended to provide an SI thyristor with a shorted cathode structure which is excellent in its turn-off characteristic, current carrying capacity and breakdown voltage, by increasing the cathode area utilization factor.

The SI thyristor of the second prior art example, which has the n^+-type cathode regions **11** and the p^+-type short-circuit regions **13** formed in one main surface of the n^--type high resistivity layer (an n^--type base region), is characterized by a construction in which the p^+-type gate regions **4** are buried in the n^--type base region **1** side by side in parallel to the said main surface thereof, the n^+-type cathode regions **11** are each formed opposite the channel region defined by the p^+-type gate regions therebetween and the p^+-type short-circuit regions **13** are disposed partly opposite the p^+-type gate regions **4**.

That is, the p^+-type gate regions **4** are provided as buried regions, the p^+-type short-circuit regions **13** are formed above the gate regions **4**, and the regions defined between the short-circuit regions **13** form the n^+-type cathode regions **11**, which serve as main current paths at the cathode side. This structure provides increased device area utilization factor.

FIG. **45** is a sectional view showing, as a third prior art example, an SI thyristor disclosed by Muraoka in Japanese Patent Public Disclosure No. 152063/85. Reference numeral **1** denotes an n^--type high resistivity layer, **3** second high concentration regions (p^+-type anode regions), **4** gate regions, *7a* a cathode electrode, *7b* a gate electrode, *7c* an anode electrode, **11** first high concentration regions (n^--type cathode regions), **12** a support electrode, and **14** and **14'** insulating regions. With such a structure as shown in FIG. **45**, the p^+-type buried gate regions **4** lessens the effect of a parasitic bipolar transistor formed in a region defined by the cathode and anode regions between them, thereby preventing retriggering of the device by the parasitic bipolar transistor, enhancing the dv/dt capability of the device immediately after its turn-off and improving the gate loss at turn-on during high-frequency operation.

The above-mentioned third prior art example is intended to offer an SI thyristor of a novel construction that is free from the parasitic bipolar transistor effect and remarkably high in the yield rate of production.

To attain such an object, in the third prior art example, the above-mentioned first high concentration regions **11** may be formed so that their junction is shallow in the regions directly above the buried regions **4** and deep in the other regions.

This structure allows the dv/dt capability just after turn-off to be held high as required, permits reduction of the gate loss at turn-on during high-frequency operation and appreciably raises the yield rate of production.

In this third prior art example, the second high concentration regions **3** may be formed so that their junction is shallow in the regions directly below the buried regions **4** and deep in the other regions. This further increases the dv/dt capability.

It is also possible to form an insulating layer between the region directly below the gate region and the anode electrode, this further enhances the above-noted effects.

In the same structure as shown in FIG. **44** of the second prior art, the inventors of this application found out a phenomenon that when the device is turned off, the p^+-type buried gate regions **4** and the p^+-type short-circuit regions **13** get shorted and extra holes are